CLAIMS

We claim:

1. A non-volatile storage device, comprising:

source/drain regions;

a channel region between said source/drain regions;

a floating gate;

a control gate;

a first dielectric region between said channel region and said floating gate, said first dielectric region includes a high-K material; and

a second dielectric region between said floating gate and said control gate, wherein charge is transferred between said floating gate and said control gate via said second dielectric region.

2. A non-volatile storage device according to claim 1, wherein:

said second dielectric region includes tunnel oxide.

3. A non-volatile storage device according to claim 1, wherein:

said second dielectric region includes silicon oxide.

4. A non-volatile storage device according to claim 1,wherein:

said control gate comprises a poly-silicon layer, a tungsten nitride barrier layer and a tungsten metal layer.

5. A non-volatile storage device according to claim 1, wherein:

said control gate includes a low resistivity layer.

6. A non-volatile storage device according to claim 1, wherein:

said first dielectric, said floating gate, said second dielectric and said control gate form a stack; and

said non-volatile storage device further comprises a first spacer at one side of said stack and a second spacer at a second side of said stack.

7. A non-volatile storage device according to claim 6, further comprising:

an oxide region surrounding said stack.

8. A non-volatile storage device according to claim 1, wherein:

said first dielectric, said floating gate, said second dielectric, and said control gate form a stack; and

said non-volatile storage device further comprises a first oxide spacer at one side of said stack and a second oxide spacer at a second side of said stack.

9. A non-volatile storage device according to claim 8, further comprising:

a first epitaxially grown silicon region adjacent said first oxide spacer; and

a second epitaxially grown silicon region adjacent said second oxide spacer.

10. A non-volatile storage device according to claim 1, wherein:

said high-K material includes Al_20_3.

11. A non-volatile storage device according to claim 1, wherein:

said high-K material includes $HfSiO_X$ or HfSiON.

12. A non-volatile storage device according to claim 1, wherein:

said high-K material includes any one of: Hafnium Silicate, Hafnium Oxide, Hafnium Silicon Oxy-Nitride, Aluminum Oxide, Zirconium Oxide, nano-laminates or suitable alloys of said above listed materials.

13. A non-volatile storage device according to claim 1, wherein:

said transferring of charge between said floating gate and said control gate includes Fowler-Nordheim tunneling.

14. A non-volatile storage device according to claim 1, wherein:

said transferring of charge between said floating gate and said control gate includes programming said non-volatile storage element by transferring electrons from said floating gate to said control gate.

15. A non-volatile storage device according to claim 1, wherein:

said transferring of charge between said floating gate and said control gate includes erasing said non-volatile storage element by transferring electrons from said control gate to said floating gate.

16. A non-volatile storage device according to claim 1, wherein:

said floating gate has rounded edges.

17. A non-volatile storage device according to claim 1, wherein:

said non-volatile storage element is a flash memory device.

18. A non-volatile storage device according to claim 1, wherein:

said non-volatile storage element is a multi-state flash memory device.

19. A non-volatile storage device according to claim 1, wherein:

said non-volatile storage element is a NAND flash memory device.

20. A non-volatile storage device, comprising:

source/drain regions;

a channel region between said source/drain regions;

a floating gate;

a control gate;

a first dielectric region between said channel region and said floating gate, said first dielectric region includes a high-K material; and

a second dielectric region between said floating gate and said control gate, said second dielectric provides for tunneling between said floating gate and said control gate in order to program said non-volatile storage device.

21. A non-volatile storage device according to claim 20, wherein:

said second dielectric region includes tunnel oxide.

22. A non-volatile storage device according to claim 20, wherein:

said first dielectric, said floating gate, said second dielectric and said control gate form a stack; and

said non-volatile storage device further comprises a first spacer at one side of said stack and a second spacer at a second side of said stack.

23. A non-volatile storage device according to claim 22, further comprising:

an oxide region surrounding said stack.

24. A non-volatile storage device according to claim 22, further comprising:

a first epitaxially grown silicon region adjacent said first spacer; and

a second epitaxially grown silicon region adjacent said second spacer.

25. A non-volatile storage device according to claim 20, wherein:

said tunneling includes programming said non-volatile storage device by transferring electrons from said floating gate to said control gate and erasing said non-volatile storage device by transferring electrons from said control gate to said floating gate.

26. A non-volatile storage device according to claim 20, wherein:

said non-volatile storage element is a flash memory device.

27. A non-volatile storage device according to claim 20, wherein:

said non-volatile storage element is a multi-state flash memory device.

28. A non-volatile storage device according to claim 20, wherein:

said non-volatile storage element is a NAND flash memory device.

29. A non-volatile storage device, comprising:

source/drain regions;

a channel region between said source/drain regions;

a floating gate;

a control gate;

means for partially electrically isolating said floating gate from said channel regions; and

means for providing a dielectric region between said floating gate and said control gate and for transferring electrons between said floating gate and said control gate.

30. A non-volatile storage system, comprising:

a set of non-volatile storage elements, each of said non-volatile storage elements includes a channel, a floating gate and a control gate, said floating gate being separated from said channel by a first dielectric region that includes a high-K material, said floating gate being separated from said control gate by a second dielectric region; and

a control circuit for programming and reading said non-volatile storage elements, said control circuit causes charge to be transferred between said floating gate and said control gate via said second dielectric.

31. A non-volatile storage device according to claim 30, wherein:

said second dielectric region includes tunnel oxide.

32. A non-volatile storage device according to claim 30, wherein:

said non-volatile storage elements include stacks wherein said first dielectric, said floating gate, said second dielectric and said control gate of each non-volatile storage element form a stack for each respective non-volatile storage element; and

said non-volatile storage device further comprises spacers on sides of said stacks.

33. A non-volatile storage device according to claim 32, further comprising:

oxide regions surrounding at least portions of said stacks.

34. A non-volatile storage device according to claim 32, further comprising:

epitaxially grown silicon regions between spacers.

35. A non-volatile storage device according to claim 30, wherein:

said control circuit causes programming of a particular non-volatile storage element by transferring electrons from a floating gate for said particular non-volatile storage element to a control gate of said particular non-volatile storage element; and

said control circuit causes erasing of said particular non-volatile storage element by transferring electrons from said control gate for said particular non-volatile storage element to said floating gate for said particular non-volatile storage element.

36. A non-volatile storage device according to claim 30, wherein:

said non-volatile storage elements are flash memory devices.

37. A non-volatile storage device according to claim 30, wherein:

said non-volatile storage elements are multi-state flash memory devices.

38. A non-volatile storage device according to claim 30, wherein:

said non-volatile storage elements are NAND flash memory devices.

39. A method of using a non-volatile storage device, comprising:

at least partially isolating a floating gate from a channel using a high-K material, said channel is between source/drain regions, said floating gate is separated from a control gate; and

programming said non-volatile storage device by transferring charge between said floating gate and said control gate.

40. A method according to claim 39, further comprising:

reading said non-volatile storage device by determining an indication of charge stored on said floating gate.

41. A method according to claim 39, wherein:

said programming includes transferring electrons from said floating gate to said control gate.

42. A method according to claim 39, wherein:

said programming includes tunneling electrons from said floating gate to said control gate.

43. A method according to claim 39, further comprising:

erasing said non-volatile storage device by transferring charge between said floating gate and said control gate.

44. A method according to claim 39, further comprising:

erasing said non-volatile storage device by transferring electrons from said control gate to said floating gate.

45. A method of making a non-volatile storage device, comprising:

depositing a high-K material over a region of a semiconductor to be used as a channel region;

depositing a floating gate over said high-K material;

adding a dielectric region over said floating gate; and

adding a control gate over said dielectric material, said non-volatile storage device is programmed by transferring charge between said floating gate and said control gate via said dielectric region.

46. A method according to claim 45, wherein:

said dielectric region includes tunnel oxide.

47. A method according to claim 45, wherein said step of adding a control gate includes:

depositing a poly-silicon layer; and

depositing a low resistivity layer above said poly-silicon layer.

48. A method according to claim 45, wherein said step of adding a control gate includes:

depositing a tungsten nitride barrier layer over said lower control gate; and

depositing a tungsten layer over said tungsten nitride layer.

49. A method according to claim 45, further comprising:

adding an epitaxially grown silicon region.

50. A method according to claim 45, wherein:

said steps of depositing a high-K material, depositing a floating gate, depositing a second dielectric, and depositing a control gate include performing any one of chemical vapor deposition, physical vapor deposition, or atomic layer deposition.

51. A method according to claim 45, further comprising:

performing sidewall oxidation, said sidewall oxidation causes rounding of edges of said floating gate and said control gate.